ECS Transactions, 16 (10) 3-12 (2008)
10.1149/1.2986748 ©The Electrochemical Society

Germanium for High Performance MOSFETs and Optical Interconnects

Krishna C. Saraswat[1], Donghyun Kim[1], Tejas Krishnamohan[1,2], Duygu Kuzum[1], Ali K. Okyay[1,3], Abhijit Pethe[1,2] and Hyun-Yong Yu.[1]
[1]Department of Electrical Engineering, Stanford University, Stanford, CA 94305, USA.
[2]Intel Corp. USA,
[3]Department of Electrical and Electronics Engineering, Bilkent University, Turkey.

It is believed that to continue the scaling of silicon CMOS innovative device structures and new materials have to be created in order to continue the historic progress in information processing and transmission. Recently germanium has emerged as a viable candidate to augment Si for CMOS and optoelectronic applications. In this work we will first review recent results on growth of thin and thick films of Ge on Si, technology for appropriate cleaning of Ge, surface passivation using high-κ dielectrics, and metal induced crystallization of amorphous Ge and dopant activation. Next we will review application of Ge for high performance MOSFETs. Innovative Si/Ge MOS heterostructures will be described with high on current and low off currents. Finally we will describe optical detectors and modulators for on-chip and off-chip interconnect. Successful integration of Ge on Si should allow continued scaling of silicon CMOS to below 22 nm node.

Introduction

For more than 30 years, the performance of Si integrated circuits has improved at an astonishing rate. It is believed that to continue the scaling innovative device structures and new materials have to be added to Si in order to continue the historic progress in information processing and transmission.

Diminishing improvement in the on current (I_{ON}) and increase in off current (I_{OFF}) may limit the scaling of bulk Si CMOS. A channel material with high mobility and therefore high injection velocity can increase on current and reduce delay. Currently, strained-Si bulk CMOS is the dominant technology and increasing the strain provides a viable solution to scaling. However, looking into future it becomes important to look at higher mobility materials like Ge together with innovative device structures to continue scaling of MOSFETs [1].

The relentless scaling paradigm is also threatened by interconnect limits including excessive power dissipation, insufficient communication bandwidth, and signal latency for both off-chip and on-chip applications. Many of these obstacles stem from the physical limitation of Cu-based electrical wires, exacerbated by the increase in copper resistivity, as wire dimensions and grain size become comparable to the bulk mean free path of electrons in Cu (~40nm). This makes it imperative to examine alternate interconnect schemes for future such as optical interconnects [2].

Recently Ge has emerged as a viable candidate to augment Si for CMOS and optoelectronic applications. First, the lower effective mass and lower valley degeneracy of Ge could alleviate the problem by providing a higher source injection velocity, which translates into higher drive current and smaller gate delay. Second, Ge has a smaller absorption coefficient, which makes it attractive for integration of monolithic optical components for the ultimate use in optical interconnects in the wavelength range of 1.3-1.55 μm commenly used in telecommunications. Third, lower processing temperatures allow 3-D integration of Ge on Si CMOS.

In this paper we will review recent results on Ge fabrication issues, including growth of Ge on Si, and surface passivation. Next we will review application of Ge for high performance nanoscale MOSFETs, optical detectors and modulators for on-chip and off-chip interconnect.

Ge Heteroepitaxial Growth on Si

Historically, Ge had been one of the most important semiconductors in the past as the first MOSFET and the integrated circuit were fabricated in Ge. Ge offers several attractive physical properties over Si. However, for Ge to become main-stream several problems need to be solved. One of the problem is that Ge substrates are not easy to handle due to its mechanical properties and it not readily available in the nature as compared to Si. Furthermore, Ge will never completely replace Si, it will augment it in special applications. The solution to this problem is heterogeneous integration of Ge on Si. In order to integrate Ge onto Si, it is pivotal to develop new methods for heteroepitaxial Ge technology because Ge growth on Si is hampered by the large lattice mismatch (4.2%). The large mismatch results in growth that is dominated by "islanding" and misfit dislocations that are formed at the Si substrate/Ge film interface terminating at the film surface as threading dislocations, thus degrading device performance.

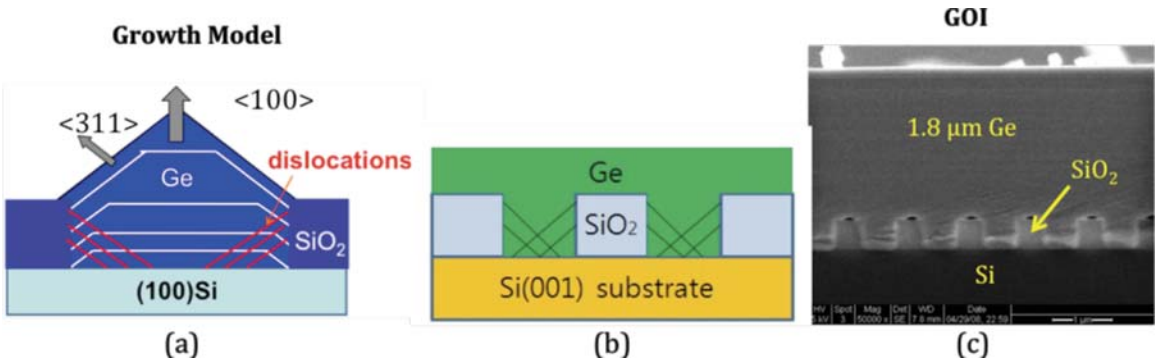


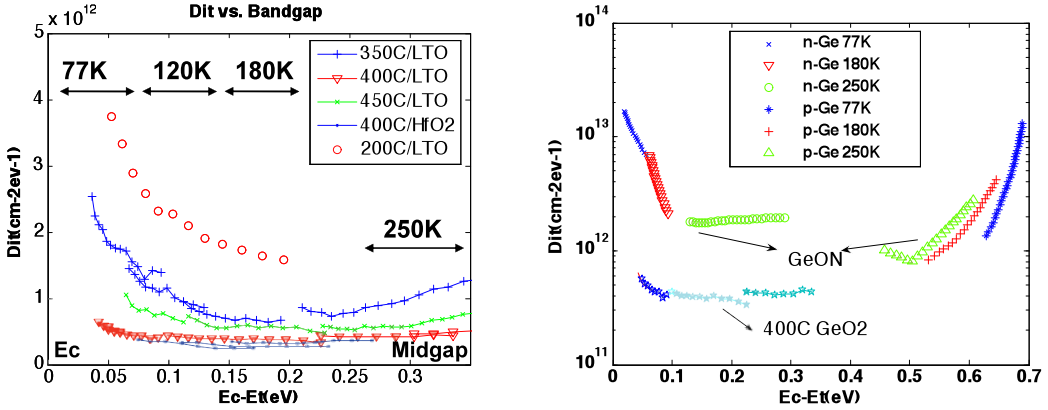
Fig. 1 Selective Ge growth on Si by *Multiple Hydrogen Annealing for Heteroepitaxy* (MHAH), (a) schematic showing direction of growth in <311> and <100> directions and threading dislocations (b) lateral overgrowth of Ge and (c) cross section TEM of a 1.5 µm Ge grown.

In our earlier work we reported on a promising approach for the monolithic integration of Ge on Si, *Multiple Hydrogen Annealing for Heteroepitaxy* (MHAH), that employs multiple cycles of growth and hydrogen anneal, for growing high quality thick heteroepitaxial Ge layers on Si substrate [3]. We now demonstrate a promising approach for the monolithic integration of Ge-based nanoelectronics and nanophotonics with Si: the selective heteroepitaxial deposition of high quality thick Ge layers Si by MHAH technique [4]. The technique involves CVD growth of a thin film of Ge on Si through openings in SiO_2 (Fig. 1) at a low temperature (~400˚C), followed by in-situ H_2 annealing at a high temperature (~825˚C) to reduce defect density and improve surface smoothness with subsequent growth of thick Ge with epitaxial lateral overgrowth on SiO_2 at a lower temperature. High quality crystalline Ge can be selectively integrated on Si platform with this technique.

Ge Surface Passivation

Ge has been considered as a promising candidate as channel material for future technology nodes because of its lower effective conductivity mass. However, passivation

of Ge interface has been a critical challenge. We demonstrated for the first time in 2002 passivation of Ge with ZrO_2 [5]. Since then surface passivation of Ge has been extensively investigated by many researchers with high-k metal oxides of Zr, Hf, Al, La, and Er. Direct formation of a high-k dielectric on Ge has not given good results in the past. In our subsequent work Ge passivation with its native oxynitride (GeO_xN_y) [6,7] and HfO_2 or ZrO_2 deposited by atomic-layer deposition (ALD) system has been studied [8]. The optimum dielectric stack could be attained by rapid thermal nitridation (RTN) of Ge in ammonia to form GeO_xN_y followed by ALD of the hi-κ film. The RTN technique was also employed to passivate the Ge surface prior to the deposition of SiO_2 for field isolation. Excellent electrical characteristics were obtained from MOSCAPs with low leakage, good C-V characteristics and reasonably low interface state density, especially for PMOS. High mobilities have been reported for Ge PMOS while Ge NMOS in the past exhibited poor drive current and low mobility by several demonstrations worldwide. To better understand the reasons of poor NMOS performance interface state density D_{it} distributions over the bandgap and close to band edges were extracted using low temperature conductance measurements. For the upper half of the bandgap, especially closer to conduction band edge, higher D_{it} values values were observed than from midgap to valence band, shown in Fig. 2.a.



(a) (b)

Fig. 2 (a) D_{it} distribution for samples ozone-oxidized in 200- 450°C range for N-type Ge substrate. Minimum Dit of 3x1011cm-2V-1 is obtained for samples grown at 400°C. At different temperatures, traps at different parts of bandgap respond. So conductance is measured at 77,120,180 and 250K to cover the bandgap. (b) D_{it} distribution for optimized GeO_2 and GeON samples.

In a major recent breakthrough we have developed a method by controlled ozone oxidation of Ge to engineer the interface significantly reduced D_{it} [7]. A minimum D_{it} of $3x10^{11}$ cm^{-2} V^{-1} was obtained for samples oxidized at 400°C in ozone ambient. Lower or higher oxidation temperatures showed increase in D_{it} values (Fig. 2.b) due to formation of Ge suboxide (GeO_x) states. Although Ge is a column IV semiconductor like Si, it behaves different from Si when oxygen or hydrogen reacts with its surface. The electrical quality of Ge interface is strongly affected by the oxidation states. With ozone engineered Ge interface capped by HfO_2 or CVD SiO_2 a minimum D_{it} of $3x10^{11}$ cm^{-2} V^{-1} is obtained (Fig. 2.b), which is in the range of state-of-the-art Si/High-K dielectric interface quality.

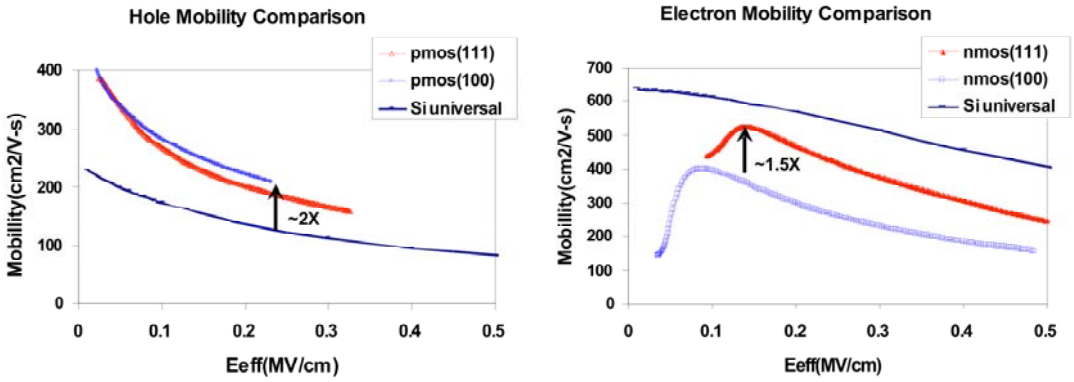
Ge MOSFETs

In Ge, the lower transport mass (m*) of electron and hole is responsible, respectively, for higher carrier mobilities μ_n and μ_p. However, native Ge oxides are either water

soluble or volatile. Ge has much smaller direct band gap giving rise to high band-to-band tunneling (BTBT) leakage. For Ge to become mainstream, surface passivation and innovative device structures to overcome must be achieved.

Bulk Ge MOSFETs

Ge MOSFETs with different dielectrics including HfO_2 [10], ZrO_2 [11], Al_2O_3 [12], $LaAlO_3$ [13], GeON have been demonstrated. Mobilities above $300cm^2V^{-1}s^{-1}$ have been reported for Ge PMOS. However, Ge NMOS exhibited poor drive current and low mobility by several demonstrations worldwide [14,15]. Better characterization of interface and understanding of mobility degradation mechanisms can be helpful to investigate the Ge NMOS problem. We have demonstrated Ge N- and P-FETs with GeON gate dielectric on (100) and (111) substrate orientations as shown in Fig. 3. We show the highest electron mobility (μ_n) for Ge NMOS reported so far and 2x improvement in hole mobility (μ_p) over Si. Also effect of substrate orientation on μ_n (electron mobility) and μ_p (hole mobility) is investigated experimentally. It is found that (111) orientation provides 50% improvement in μ_n over (100) orientation. Carrier scattering mechanisms and their effect on μ_n and μ_p are studied through low temperature electrical characterization. Coulomb scattering is found to be the prominent degradation mechanism for μ_n while the effective scattering mechanism for holes is phonon scattering. Ge-GeON interface is further investigated using conductance technique at low temperatures to get accurate distribution of D_{it} across the bandgap of Ge.



(a) (b)

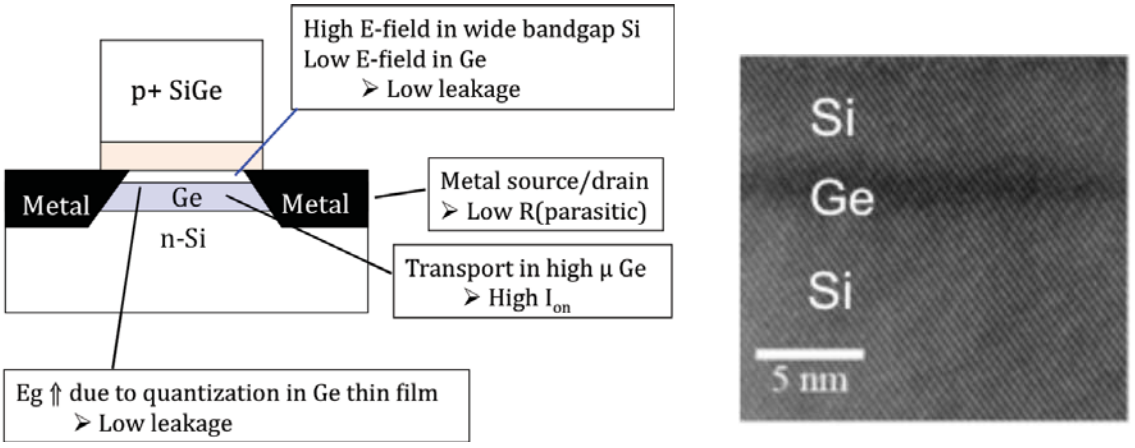
Fig. 3 Mobility vs. effective field for GeON gate dielectric MOSFETs on (111) and (100) Ge surface orientations (a) PMOS Hole mobility shows 2x improvement over universal Si mobility, (b) highest electron mobility to-date for NMOS.

Strained Si/Ge/Si Heterostructure FET (H-FET)

Straining Ge and Si_xGe_{1-x} can significantly increase μ_p because of a reduction in m* and the band splitting due to strain. In extremely scaled MOSFETs, the relation between the short-channel I_{on} and μ is not direct or obvious. Through detailed band-to-band-tunneling (BTBT) (including band structure and quantum effects), Full-Band Monte-Carlo and 1-D Poisson-Schrodinger simulations on ultra-thin, nanoscale double gate FET structures, we have systematically compared different high mobility channel materials in terms of the drive current, intrinsic delay and off-state leakage [16,17].

The materials such as strained Si and strained Ge and many III-V materials, have larger carrier mobility than silicon, but the enhanced leakage because of their smaller bandgap or direct band gap may limit their scalability. In a nanoscale transistor generally

the minimum standby off-state currents ($I_{OFF,min}$) is determined by the BTBT leakage, I_{BTBT} [18]. The leakage current for strained-Si increases monotonically with increasing strain due to the rapid reduction in the E_G and m*, whereas the dependence of I_{OFF} for strained-Ge is not monotonic and reveals an optimum point of minimum leakage [8].



(a) (b)

Fig. 4. (a)Schematic of the Si/s-Ge/Si hetero-structure FET (H-FET), (b) cross section TEM of the channel region.

Strain in general results in reduction in the E_G and hence enhanced I_{BTBT}. Confinement on the other hand results in increased E_G and hence reduced I_{BTBT}. The heterostructure FET of Fig. 4 proposes a novel device structure to combine strain and quantum mechanical confinement to obtain desired transport properties with reduced off-state leakage. In these structures the transport can be confined to the center of the channel in a high mobility material flanked by a high E_G material. The mobility is further enhanced due to strain, reduced electric field in the center of the channel and the channel being away from the dielectric interface. The bandgap of the center channel can be increased due confinement by keeping it very thin.

We have demonstrated [1,20,21] a novel Si/s-Ge/Si hetero-structure FET (H-FET), in which the transport occurs in high μ_p s-Ge and leakage in wider E_G Si (**Fig. 4**). This reduces the I_{BTBT}, while retaining high μ_p of Ge (**Fig. 5)**. The confinement of thin Ge between Si results in an increase in the E_G and hence reduction in I_{BTBT}, while strain keeps μ_p high. Experimentally, the resulting optimal structure obtained was an ultra-thin, low defect, fully strained Ge epi channel on relaxed Si (r-Si). H-FETs on bulk Si show a ~2X μ_p enhancement over Si, while H-FETs on SOI show even higher μ enhancements of >4X over Si [20]. Both types of H-FETs show reduction in I_{OFF} compared to bulk Ge devices. In particular H-FETs on SOI show significant reduction in I_{OFF} due to reduced E-field in Ge and Eg increase due to confinement.

In a simulation study we have investigated the performance of a nanoscale HFET double gate PMOS structure and compared it to conventional relaxed and biaxial strained Ge and Si channel structure [18,20]. The non-local empirical pseudopotential method (bandstructure), full-band Monte-Carlo simulations (transport), 1-D Poisson-Schrodinger (electrostatics) and detailed band-to-band-tunneling (BTBT) (including bandstructure and quantum effects) simulations, the effect of biaxial-strain, band-structure, mobility, effective masses, density of states, and high-field transport on the drive current, off-state leakage and switching delay in nano-scale, Si, SiGe and Ge, p-MOS DGFETs was

thoroughly and systematically investigated. Fig. 5 shows summary of this work comparing L_G=15nm, T_{body}=5nm, T_{OX}=1nm clearly illustrating the efficacy of the HFET.

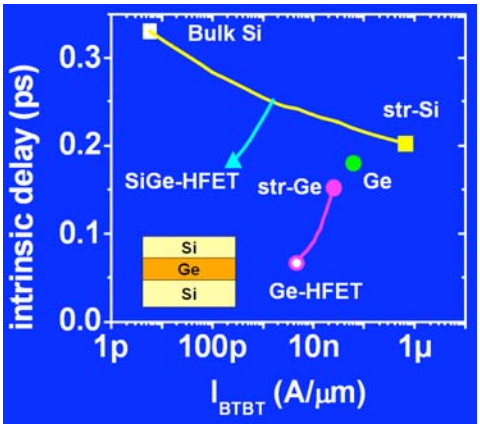


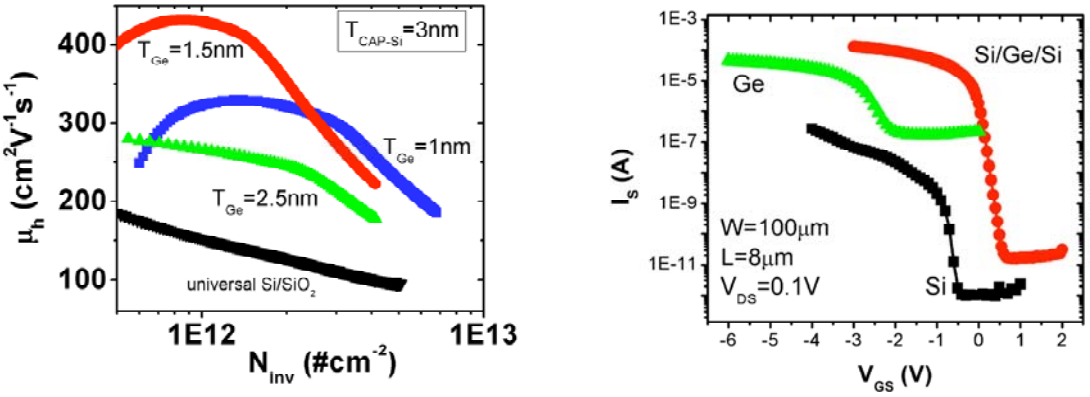
Fig. 5. Tradeoff associated with changing the channel materials in a double gate PMOS with L_G=15nm, T_{body}=5nm, T_{OX}=1nm. The BTBT limited OFF current is plotted against the intrinsic switching speed of the device. SiGe HFET is assumed to have 60% Ge.

Metal Source/Drain

Parasitic resistance in the S/D regions of the conventional MOSFET has been identified as one of the primary problems of the non-scaling of drive currents in transistor scaling. Replacing the S/D regions of transistors with metals has been suggested as one of the techniques, which might help reduce this effect. Use of the metal S/D offers additional advantages of low-temperature processing for S/D formation, elimination of the parasitic bipolar action and inherent physical scalability of the gate lengths due to the abrupt silicide-silicon interface. However, for the I_{ON} of the metal S/D to be better than diffused S/D the Schottky barrier to channel needs to be very small. In the case of Ge we have found that the the Fermi level at metal-Ge Schottky barriers is pinned near the valence band of Ge for a variety of metals, including, Ni, Co and Ti [21]. The free-electron wavefunction penetrates from the metal into the semiconductor, which generates metal-induced gap-state (MIGS) and pins the Fermi level. Since Ge has smaller bandgap and higher dielectric constant than Si, the strong Fermi level pinning occurs near charge neutrality level (E_{CNL}) which is close to the valence band. This provides a very small barrier to the holes in the channel in a PMOS and a large barrier to the n-type substrate. Due to the small barrier height to holes coupled with the high inversion hole mobility, Schottky S/D Ge transistors provide for very high drive currents. We have built high performance PMOSFETs on Si substrates using a Si/Ge/Si heterostructure channel and NiSi Source/Drain regions [21]. Schematic of the transistor is shown in Fig. 4. Excellent PMOS characteristics were achieved when the doped S/D region in Ge transistors was replaced with metallic NiGe. Using a thin Ge layer within the inversion region of a Schottky Si – PMOSFET provides for higher hole mobility (~2X), as shown in Fig. 6, and much higher drive currents due to almost zero barrier height to holes in the channel. Also the OFF state leakage is maintained at a low value because it is limited by the large barrier height in the wider bandgap Si and Ge quantization. The transistor hence, combines the advantages of high mobility, and low parasitic resistance and is an attractive candidate for scaling PMOSFETs into the sub-20nm regime.

Since strong Fermi level pinning occurs near charge neutrality level (E_{CNL}) which is close to the valence band, and thus high Schottky barrier height to n-Si is known to be a

serious problem for NMOSFETs. Recently we have demonstrated Schottky barrier height modulation in metal/Ge Schottky junctions by inserting an ultrathin interfacial SiN layer [VLSI 08]. The ultrathin insulator inserted between metal/Ge interface blocks the free state penetration into Ge and equivalently reduces MIGS density. As a result, Fermi level pinning is released and the Schottky barrier height to n-Si becomes a function of metal workfunction. Nearly zero Schottky barrier height was successfully obtained for electrons. We applied this technology to demonstrate metal S/D Ge NMOSFETs.



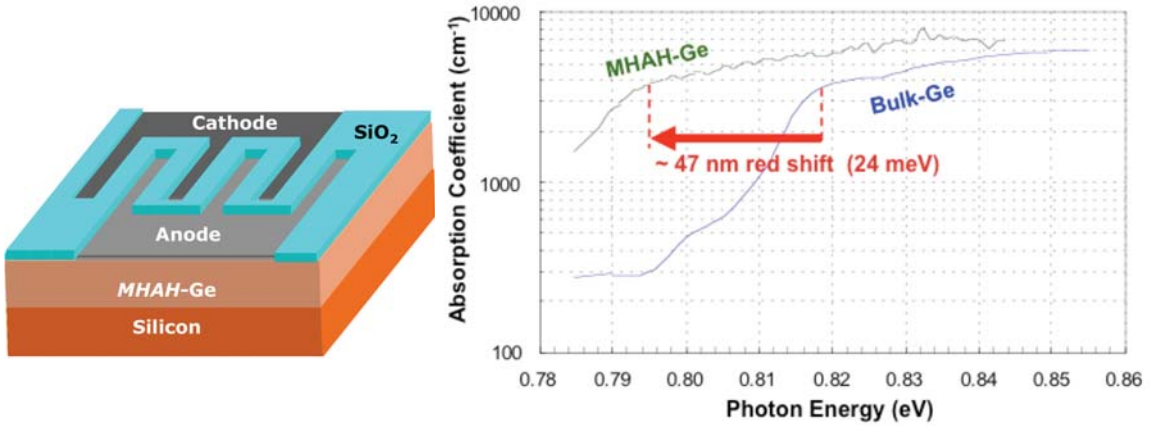
(a) (b)

Fig. 6 (a) Hole mobility in biaxial strained Si/Ge/Si Schottky S/D HFETs for fixed cap Si thickness T_{capSi} and varying Ge thickness T_{Ge}, and (b) I_S vs. V_{GS} for Ge, Si and biaxial strained Si/Ge/Si Schottky S/D HFETs.

Ge based Photonics for Optical Interconnects

The communications bottleneck is identified as one of the grand challenges in the progress of silicon computation. While individual logic elements have become significantly faster, computational speed is limited by the communication between different parts of a processor. Traditional copper wires are efficient at short distances, but they suffer excessive power dissipation and delay in global lines, and cannot cope with the ever growing bandwidth demand. Moreover, with the chip architectures evolving towards a modular design, the requirements for increased bandwidth density further strain the electrical interconnects. Optical interconnects can provide a solution to the communication bottleneck by alleviating significant power dissipation and delay problems faced by copper wires [2,22]. Monolithically integrated photodetectors and optical modulators with very low capacitance are among the essential elements needed for high performance optical interconnects.

Ge has been emerging as a viable candidate for integration with Si for low-cost transceivers to overcome the spectral limit of Si photodetectors which are not efficient at wavelengths (1.3-1.55 mm) for medium- and long-haul optical fiber communications due to the inherent large bandgap of Si. We have successfully demonstrated metal-semiconductor-metal (MSM) photodetectors in Ge grown directly on Si using the MHAH technique that allows growth of high quality thick heteroepitaxial-Ge layers on Si, as shown in Fig. 7(a). [23]. An important byproduct of this growth technique is tensile strain within the Ge film, resulting in enhanced absorption around 1550 nm, as shown in Fig. 7(b). Up to 68% quantum efficiency detectors with 0.85 A/W responsivities were achieved at 1550 nm. Exceptionally high efficiency of the photodiodes at 1.55 mm also reveals the high quality of the grown *MHAH*-Ge layers. This technology is promising to realize monolithically integrated optical links as an alternative to electrical interconnects.



(a) (b)

Fig. 7. (a) Schematic of the MSM photodetector in ! "#" $%&' ( ) Ge on Si technique, (b) *+,*&-. *) /01203 4' &, /-') 25' *66-5-*) /278$_{Ge}$9:4;2,<' /') 2*) *&%=26' &2! "#" $%&' ( ) 2>*2 10=*&4;2$B_{Ge}$-42*+/&05/*?26&' . 2. *04@&*?2&*4,') 4-:-/=25' &&*5/-) %26' &24@&605*2&*61*5/-') 42 0) ?2044@. -) %2ABC 2-) /*&) 012D@0) /@. 2*66-5-*) 5=;2E<*2034' &, /-') 25@&:*26' &2&*10+*?2>*2 -42014' 2,1' //*?26' &2&*6*&*) 5*2,@&,'4*4;2#2FG2) . 2&*?24<-6/2' 62/<*2034' &, /-') 2*?%*2-42 &*5' &?*?2?@*2/' 2/*) 4-1*2train.

We have introduced a SiGe switching device that can perform optoelectronic conversion at the nanoscale [24]. This optoelectronic switch is a fusion of a Ge optical detector and a Si MOSFET, as depicted in Fig. 8. Signal is generated remotely and is transmitted as optical energy in the 1330-1550nm window where Ge is a strong absorber. Optically generated carriers move within the gate due to band bending and the applied gate bias. This constitutes a gate current which in turn modifies the channel electrostatics, inducing a highly amplified drain current. Si, however, is transparent at these wavelengths, so no absorption takes place in the channel; hence the surrounding Si circuitry is noise free, providing noise immunity from signaling. As light is turned off, the gate oxide capacitance discharges through both increased recombination in the gate depletion region and diffusion due to gradient in the carrier concentration. The speed of the device is limited by turn-off which can be controlled by carrier lifetimes and thickness of the polycrystalline gate region. The use of Ge enables operation in the standard telecommunication wavelengths in the 1330-1550nm window in addition to providing the surrounding Si circuitry with noise immunity from signaling. The transconductance of the FET provides amplification and experimental current gain of up to 1000× is demonstrated. Plasmonic coupling could be used to focus light on such nano-scale dimensions by nano-metallic structures to further enhance device performance [nature paper]. The switch can be fabricated at the nanoscale along with high performance Si CMOS. Very low capacitance can be achieved due to isolation of detection region from the current drive. Optoelectronic conversion performed with such a compact device offers the potential of inserting light at the latch level in a processor. The switch may be used as an optical latch to distribute an optical clock on the chip, eliminating the power dissipation and area due to an H-tree clock distribution network.

In a sister group at Stanford observations of quantum-confined Stark effect electroabsorption in Ge quantum wells with SiGe barriers grown on Si substrates has been observed [25]. An electroabsorption modulator on a Si substrate based on the quantum confined Stark effect in strained Ge quantum wells with SiGe barriers has been

demonstrated (Fig. 9). Though Ge is an indirect gap semiconductor, the resulting effects are at least as clear and strong as seen in typical III-V quantum well structures at similar wavelengths. The effect can be seen around 1550nm wavelength. This effect is very promising for practical high-speed, low-power optical modulators fabricated compatible with mainstream silicon electronic integrated circuits.

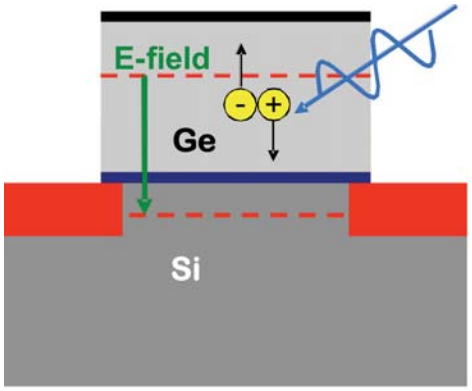


Fig. 8. Schematic of the novel optoelectronic MOSFET switch.

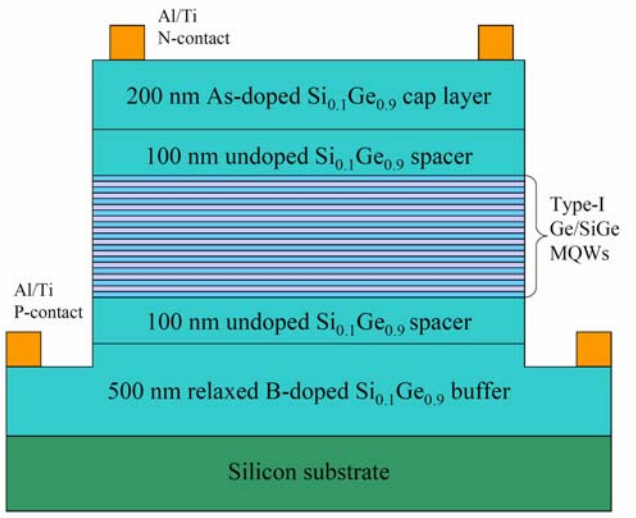


Fig. 9. Schematic of the electroabsorption modulator based on quantum-confined Stark effect [25].

Summary

Innovative device structures and new materials must be considered to continue the historic progress in information processing and transmission. Ge has emerged as a viable candidate to augment Si for CMOS and optoelectronic applications. As a promising MOSFET channel material candidate, Ge offers numerous advantages over Si. In this work, we have addressed the classic problems of Ge surface passivation and its incorporation on Si, and demonstrated various advanced Ge MOSFETs appropriate for nanoscale technologies. We have demonstrated Ge optical detectors and modulators integration on Si for on-chip and off-chip interconnect in the standard telecommunication wavelengths in the 1330-1550nm window.

Acknowledgments

The work described here was performed at Stanford University and supported by MARCO MSD and IFC Focus Centers, DARPA, and Stanford University INMP program. The authors would like acknowledge important contributions of his students and colleagues: C. O. Chui, J. Harris, P. C. McIntyre, D. Miller, A. Nayfeh, and Y. Nishi

References

1. K. C. Saraswat, C. O. Chui, T. Krishnamohan and A Pethe, *IEEE IEDM Digest,* p. 659, 2006.
2. K.-H. Koo, H. Cho, P. Kapur, and K. C. Saraswat, *IEEE Trans. Electron Dev.*, **Vol. 54**, No. 12, pp. 3206-3215, Dec. 2007.
3. A. Nayfeh, C. O. Chui, . K. C. Saraswat and T. Yonehara, *Appl. Phys. Lett.,* **Vol. 85**, No. 14, pp. 2815-2817, 4 Oct. 2004

4. Hyun-Yong Yu, Jin-Hong Park, Ali K. Okyay,and K. C. Saraswat, *This symposium*.
5. C. O. Chui, H. Kim, D. Chi, B. B. Triplett, P. C. McIntyre and K. C. Saraswat, *IEEE IEDM Tech. Dig.*, p. 437, 2002.
6. C. O. Chui, F. Ito and K. C. Saraswat, *IEEE Trans. Electron Dev*. **vol. 53**, no. 7, pp. 1501-1508, 2006.
7. A. Pethe and K. C. Saraswat, *IEEE SISC,* Dec. 2006
8. C. O. Chui, H. Kim, D. Chi, Paul C. McIntyre and K. C. Saraswat, *IEEE Trans. Electron Dev*. **vol. 53**, no. 7, pp. 1509-1516, 2006.
9. 7. D. Kuzum, et al., *IEEE IEDM*, 2007, p. 723
10. E. P. Gusev, H. Shang, M. Copel, M. Grilbeyuk, C. D'Emic, P. Kozlowski, T. Zabel, App. Phys. Lett., **85**, 2004, pp.2334-2337
11. C. O. Chui, S. Ramanathan, B. B. Triplet, P. C. McIntyre, K. C. Saraswat, *IEEE Elec. Dev. Lett.,* **23**, 2002, pp. 473-476
12. S. Iwauchi, T. Tanaka, *Jpn. J. Appl. Phys*., **10**, 1971, pp.260-265
13. D. S. Yu, K. C. Chiang, C. F. Cheng, A. Chin, C. Zhu, M. F. Li, D-L. Kwong, *IEEE Elec. Dev. Lett.,* **25**, 2004, pp. 559-562.
14. H. L. Shang, H. Okorn-Schmidt, K. K. Chan, M. Copel, J. A. Ott, P. M. Kozlowski, S. E. Steen, S. A. Cordes, H.-S. P. Wong, E. C. Jones, and W. E. Haensch, Proc. IEDM, 2002, pp.441–444.
15. H. Shang, K-L. Lee, P. Kozlowski, C. D'emic, I. Babich, E. Sikorski, M. Ieong, H.-S. P. Wong, K. Guarini, W. Haensch, IEEE Elec. Dev. Lett., **25**, 2004, pp.135-138.
16. T. Krishnamohan, Z. Krivokapic, K. Uchida, Y. Nish and K. C. Saraswat, *IEEE Trans. Electron Dev.*, **Vol. 53**, No. 5, May 2006, pp. 990-999.
17. D. Kim, T. Krishnamohan, K. C. Saraswat, *IEEE Dev. Res. Conf*., June 2008.
18. D. Kim, T. Krishnamohan, Y. Nishi and K. C. Saraswat, *IEEE SISPAD,* Monterey, p. 389, Sep 2006
19. T. Krishnamohan, Z. Krivokapic, K. Uchida, Y. Nish and K. C. Saraswat, *IEEE Trans. Electron Dev*., **Vol. 53**, No. 5, May 2006, p. 990.
20. T. Krishnamohan, C. Jungemann, D. Kim, E. Ungersboeck, S. Selberherr, P. Wong, Y Nishi and K. C. Saraswat, *IEEE IEDM Digest*, p. 937, 2006.
21. A. Pethe and K. C. Saraswat, *IEEE Dev. Res. Conf,* June 2007.
22. H. Cho, P. Kapur, and K. C. Saraswat, *IEEE J. Lightweight Tech*., **Vol. 22**, pp. 2021-2033, Sept. 2004.
23. Ali K. Okyay, A. M. Nayfeh, T. Yonehara, A. Marshall, P. C. McIntyre and K. C. Saraswat, *Optics Letters,* **Vol. 31**, Issue 17, pp. 2565-2567 (2006).
24. A. K. Okyay, A. J. Pethe, D. Kuzum, S. Latif, D. A. B. Miller, and K. C. Saraswat, *Optics Letters,* **Vol. 32**, Issue 14, pp. 2022-2024 (2007).
25. J. E. Roth, O. Fidaner, R. K. Schaevitz, Y. -H. Kuo, T. I. Kamins, J. S. Harris, and D. A. Miller, *Opt. Express,* **15**, pp. 5851-5859, 30 April, 2007